AF/2826

Patent

Attorney's Docket No. 026350-028

#16 Appeal Brief Board 7/19/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
Toshiro HIRAMOTO et al.	)	Group Art Unit: 2826
Application No.: 09/389,321	)	Examiner: T. Dickey
Filed: September 3, 1999	)	Appeal No.
For: MOS TRANSISTOR WITH A CONTROLLED THRESHOLD VOLTAGE	)	Confirmation No: 5290

BRIEF FOR APPELLANT

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: June 18, 2002

Sir:

This is an appeal from the decision of the Primary Examiner dated October 19, 2001 (Paper No. 11). In the Office Action, the Examiner stated that claims 1-12 were rejected under 35 U.S.C. § 103. Claims 1-12 are reproduced in Appendix A to this Brief. In addition, Appendix B contains Figures 5-11 and Appendix C contains a comparison of the prior art and the present invention.

A check covering the [X] $160.00 (220) [ ] $320.00 (120) Government fee and two extra copies of this brief are being filed herewith.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in triplicate.

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I. Real Party in Interest

The present application is assigned to the University of Tokyo who is the real party of interest.

II. Related Appeals and Interferences

There are no known currently pending related appeals or interferences in the subject application.

III. Status of Claims

Claims 1-12 remain pending in the subject application.

IV. Status of Amendments

A response to the Office Action dated October 19, 2001 was filed on April 19, 2002 traversing the Examiner's rejection. No amendments were made to the claims in the April 19, 2002, response.

V. Summary of the Invention

It is an object of the present invention to provide a MOS transistor with a threshold voltage and a method of controlling a threshold voltage of a MOS transistor which are capable of operating the circuit including such a MOS transistor at higher speed and reducing a power consumption of the circuit including such a MOS transistor. (page 4, lines 20-24)

Fig. 5 is a schematic diagram showing a first embodiment of the MOS transistor according to the present invention. In the embodiment, a n type SOI MOS transistor is used as the MOS transistor. The SOI MOS transistor comprises a SOI 23 which has a substrate 20 composed of a silicon, a single crystal layer 21 composed of a single crystal silicon and an insulating layer 22 interposed between the substrate 20 and the single crystal layer 21. The insulating layer 22 is composed of SiO_2. (page 8, lines 17-23)

The single crystal layer being formed therein with a n type source region 24, a n type drain region 25 and a body 26 as the surrounded region surrounded by the source region 24 and the drain region 25. The body 26 includes a depletion layer having a composition surface which is in contact with the insulating layer 22. A gate oxide 28 is interposed between the body 26 and a gate electrode 27. (page 8, line 24 through page 9, line 1)

In the embodiment, the substrate 20 is subjected to apply a negative voltage V_{sub1} as the voltage of the first polarity. Such a voltage V_{sub1} is applied from outside of a LSI, or is applied after producing it in a circuit including the MOS transistor. (page 9, lines 2-5)

The operation of the embodiment will be described. When the negative voltage V_{sub} is adapted to be applied to the substrate 20, electrons are introduced into the substrate 20. That is, a p type neutral region (i.e. holes) which is not present in the conventional fully depleted SOI MOS transistor is provided in the body 26 electrically by the voltage V_{sub}. The MOS transistor having such a structure is referred to an Electrically Induced Body MOS (EIB-MOS) transistor. (page 9, lines 6-11)

As a result, the depth of the depletion layer corresponds to a depth t_{SOI2} of the single crystal layer 21 because there are holes over a composite surface of the body 26. The body effect factors γ of the SOI MOS transistor as shown in Fig. 5 is expressed as the following equation.

$$\gamma \fallingdotseq 3t_{fox3}/t_{SOI2} \qquad (4)$$

Wherein t_{fox3} is a thickness of a gate oxide 28. This body effect factors γ is not dependent on an impurity concentration of the body. In accordance with the embodiment, therefore, the body effect factors γ can be determined without being dependent on the impurity concentration of the body, and it is understood that the body effect factors γ increases as t_{SOI2} becomes smaller. As a result, it is possible to operate the circuit including the MOS transistor at higher speed and reduce a power consumption of the circuit including the MOS transistor. When the MOS transistor is applied in VTMOS

technique as described hereinafter, a large threshold voltage shift can be obtained with small body voltage shift. Therefore, it is possible to operate the circuit including the VTMOS transistor at high speed in an active mode, and to reduce a leakage current. (page 9, lines 12-28)

Fig. 6 is a schematic diagram showing a second embodiment of the MOS transistor according to the present invention. In the embodiment, a n type inversion mode DTMOS transistor 29 is used as the MOS transistor. A substrate of the DTMOS transistor 29 is adapted to apply a negative voltage V_{sub2}. The MOS transistor as shown in Fig. 6 performs a similar operation with that of the MOS transistor as shown in Fig. 5. (page 10, lines 1-6)

Fig. 7 is a schematic diagram showing a third embodiment of the MOS transistor according to the present invention. In the embodiment, a n type accumulation mode DTMOS transistor 30 is used as the MOS transistor. The accumulation mode DTMOS transistor 30 has a channel which is doped with impurities so that the channel has the same conductive type (in this case, n type) as that of carriers introduced into the channel. A substrate of the DTMOS transistor 30 is adapted to apply a negative voltage V_{sub3}. According to the embodiment, as described below, it is possible to lower the threshold voltage while the body effect factors γ increases remarkably, and a compromise of the fast operation and the reduction of the power consumption can be improved much more. (page 10, lines 7-17)

Fig. 8 is a schematic diagram showing a fourth embodiment of the MOS transistor according to the present invention. In the embodiment, a CMOS circuit 31 is formed with a n type inversion mode DTMOS transistor and a p type inversion mode DTMOS transistor. Each of substrates of the n type inversion mode DTMOS transistor and the p type inversion mode DTMOS transistor is adapted to apply negative voltage V_{sub4} and positive voltage V_{sub5}, respectively. The circuit as shown in Fig. 8 performs a similar operation with that of the circuit as described. (page 10, lines 18-25)

Fig. 9 is a schematic diagram showing a fifth embodiment of the MOS transistor according to the present invention. In the embodiment, a CMOS circuit 32 is formed with a n type accumulation mode DTMOS transistor and a p type accumulation mode DTMOS

transistor. Each of substrates of the n type accumulation mode DTMOS transistor and the p type accumulation mode DTMOS transistor is adapted to apply negative voltages V_{sub6} and V_{sub7}, respectively. The MOS transistor as shown in Fig. 9 performs a similar operation with that of the MOS transistor as described. (page 10, line 26 through page 11, line 5)

Fig. 10 is a schematic diagram showing a sixth embodiment of the MOS transistor according to the present invention. The MOS transistor as shown in Fig. 10 comprises an EIB-VTMOS (EIB-variable-threshold MOS) transistor 41 which has a NMOS region 41 a and a PMOS region 41b. Each of substrates of the NMOS region 41 a and the PMOS region 4 lb is adapted to apply well voltages V_{nwell1} and V_{pwell1} in addition to a negative voltage V_{sub8} and a positive voltage V_{sub9}, respectively. The nMOS region 41a and the PMOS region 41b are not fully isolated from each other by an insulating section 42 electrically. (page 11, lines 6-14)

Fig. 11 is a schematic diagram showing a seventh embodiment of the MOS transistor according to the present invention. In the embodiment, an EIB-VTMOS transistor 43 has a nMOS region 43a and a pMOS region 43b which are fully discrete from each other by an insulating section 44 electrically. In this case, also, each of substrates of the nMOS region 43a and the pMOS region 43b is adapted to apply well voltages V_{nwell2} and V_{pwell2} in addition to a negative voltage V_{sub10} and a positive voltage V_{sub11}, respectively. (page 11, lines 15-21)

VI. The Issues

The issued presented for review are:

a) whether claims 1, 2, 4-6, 7, 8 and 10-12 were properly rejected under 35 U.S.C. § 103 as being unpatentable over *Burr* (U.S. Patent No. 6,100,567); and

b) whether claims 3 and 9 were properly rejected under 35 U.S.C. § 103 as being unpatentable over *Burr* in view of *Warashina et al.* (U.S. Patent No. 5,698,885).

VII. Grouping of Claims

It is respectfully submitted that claims 2-5 and 8-11 do not stand or fall together with claims 1, 6, 7 and 12 since it is respectfully submitted that claims 2-5 and 8-11 recite additional features which are separately patentable as discussed below.

VIII. Applicants arguments against the rejection of claims 1, 2, 4-6, 7, 8 and 10-12 under 35 U.S.C. § 103

A. Errors in the Rejection

It is respectfully submitted that the rejection of claims 1-2, 4-8 and 10-12 is erroneous because the difference between the claimed subject matter and the cited prior art is such that the invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. It is respectfully submitted that the Examiner is only selecting bits and pieces from the reference without considering the remaining teachings of that reference which would lead away from the claimed invention. Furthermore, it is respectfully submitted that the Examiner is misinterpreting *Burr* and impermissibly modifying thereof in light of Applicants' teachings.

B. Limitations Not Described in the Prior Art

One limitation not described in the prior art is that the body or surrounded region includes a depletion layer having a composition surface which is in contact with the insulating layer as claimed in claims 1, 6, 7 and 12. An additional feature not disclosed in the prior art is that the MOS transistor comprises an EIB-MOS transistor as claimed in claims 1, 6, 7 and 12. A third feature not disclosed by the prior art is that the substrate of the EIB-MOS transistor is applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the body or surrounded region as claimed in claims 1, 6, 7 and 12.

An additional limitation not described in the prior art is that the EIB-MOS transistor comprises a EIB-DTMOS transistor as claimed in claims 2 and 8.

A further limitation not described in the prior art is that the EIB-MOS transistor comprises a EIB-VTMOS transistor as claimed in claims 4 and 10. An additional limitation not described in the prior art is that the MOS transistor is included in a CMOS circuit as one of a pair of EIB-MOS transistors as claimed in claims 5 and 11.

C. Explanation of Why the Limitations Render the Claimed Subject Matter Unobvious Over the Prior Art

Burr appears to disclose a fully depleted silicon-on-insulator (SOI) device which includes an intrinsic channel region and a mechanism for tuning the threshold voltage thereof. (col. 1, lines 9-12) A "fully depleted" SOI device is shown in FIG. 3. Here, the device is configured such that the depletion regions 328 extend completely down to the interface with the oxide layer 308. The structure is otherwise similar to that of the partially depleted device, and includes an nfet 302 having source and drain n-regions 312 and 314, a p-type channel region 316, and a gate 318, and a pfet 304 having source and drain p-regions 320 and 322, an n-type channel region 324, and a gate 326. The substrate 310 is tied to a fixed potential such as ground. (col. 1, lines 48-59) Another configuration that has been proposed is shown in FIG. 5. Here, a first buried back gate p+ well 540 is formed within a p- substrate 510 beneath the nfet 518 (having n-type source and drain regions 512 and 514, a p-type channel region 516, and a gate 518), and a second buried back gate n+ well 542 is formed within the p- substrate beneath the pfet 504 (having p-type source and drains regions 520 and 522, an n-type channel region 524, and a gate 526). By providing separate contacts 544 and 546 in the conductive regions 540 and 542, respectively, separate bias potentials can be applied to the nfet 502 and pfet 504, thereby tuning the threshold voltage of each device. This approach has the advantage of avoiding the extra layers needed for the SOI AS structure, but suffers the drawback that it is only possible to decrease the threshold voltages slightly before forward biasing the p-n junction between the nfet and pfet back-gate wells, and thus the configuration of FIG. 5 cannot significantly reduce the threshold voltage, especially at low supply voltages. Further, the design is constrained by the diode leakage between the p and n conductive regions 540 and

542. For example, in the case where n-well bias potential is 0.6 volts less than the p-well bias potential, about 1 μA per micron of leakage will be present. These drawbacks are particularly acute for standard threshold devices when it is desired to reduce the threshold to an extremely low value. (col. 2, line 46 through col. 3, line 4)

Thus, *Burr et al.* merely discloses a prior art device such as shown in Figure 4 of the present application and in particular *Burr* merely discloses a fully depleted SOI device in which the depletion region 328 extends completely down to the interface of the oxide layer 308. Thus, nothing in *Burr* shows, teaches or suggests a surrounded or body region including a depletion **layer** having a composition surface which is in contact with the insulating layer as claimed in claims 1, 6, 7 and 12. Rather, *Burr* merely discloses a depletion region 328.

Additionally, nothing in *Burr* shows, teaches or suggests a EIB-MOS transistor as claimed in claims 1, 6, 7 and 12. Applicants respectfully point out that the Examiner has admitted that EIB, electrically induced body and EIB-MOS are terms which cannot be found outside of Applicants' work. However, the Examiner then goes on to misinterpret what this means contrary to what is stated in the specification on page 9, lines 6-28. In the amendment filed August 7, 2001, Applicants tried to point out to the Examiner that his interpretation of a EIB was incorrect. Furthermore, in the amendment filed August 19, 2002, the Applicants provided the Examiner with four references to provide definitions of a EIB.

Burr merely discloses controlling the threshold voltages in accordance with the substrate bias. However, as claimed in claims 1, 6, 7 and 12, a voltage of a first polarity applied to the substrate of the EIB-MOS transistor induces charges of a second polarity over the composition surface of the surrounded or body region. Below, please find a chart which shows the differences between the present invention and *Burr*.

	state of SOI back interface	substrate bias (Vsub)	body bias (Vbody)
Present Invention	inversion or accumulation	constant	variable
BURR	depletion	variable	non-variable because body is depleted.

In particular, in the present invention as claimed in claims 1, 6, 7 and 12, the threshold voltage is controlled by changing the body potential of the MOS transistor where the body potential is changed based upon the voltage applied to the substrate and thus is changed by the amount of charge induced over the composition surface of the body region. However, *Burr* merely discloses that the threshold voltage is controlled in accordance with the substrate bias. In other words, the voltage applied to the substrate of the EIB-MOS transistor in the invention as claimed in claims 1, 6, 7 and 20 is not used to control the threshold voltage, but is used for forming the surrounded or body region electrically.

D. Why the Reference Taken as a Whole Does Not Suggest the Claimed Invention and Why the Features Disclosed in the Reference May Not Be Modified as Suggested by the Examiner

As discussed above, nothing in *Burr* shows, teaches or suggests a) a surrounded or body region including a depletion layer having a composition surface which is in contact with the insulating layer, b) a EIB-MOS transistor or c) the substrate of the EIB-MOS transistor is applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the surrounded or body region as claimed in claims 1, 6, 7 and 12.

Furthermore, the Examiner contends that by placing an insulator between the transistor body and gate in *Burr*, a composition surface is formed such that the depletion layer surface is in contact with the insulating layer and thus one skilled in the art would

understand that applying a voltage to the conductive substrate would cause all surfaces, including the one opposing the composition surface to have that voltage. However, Applicants respectfully traverse the Examiner's characterization of *Burr* and the present invention. Applicants respectfully bring the Board's attention to Appendix C which shows the difference between the present invention and *Burr*. In particular, as shown in (a) of Appendix C, the present invention has ten electrodes including NMOS gate electrode 1, nMOS source electrode 2, nMOS drain electrode 3, nMOS body electrode (Vbody1) 4, nMOS substrate electrode (Vsub1) 5, pMOS gate electrode 6, pMOS source electrode 7, pMOS drain electrode 8, pMOS body electrode (Vbody2) 9, and pMOS substrate electrode (Vsub2) 10. In contrast as shown in (b) in Appendix C, the MOS transistor according to *Burr* has only eight electrodes, that is, nMOS gate electrode 21, nMOS source electrode 22, nMOS drain electrode 23, nMOS substrate electrode (Vsub1) 24, pMOS gate electrode 25, pMOS source electrode 26, pMOS drain electrode 27 and pMOS substrate electrode (Vsub2) 28. Thus, nothing in *Burr* shows, teaches or suggests the features as claimed in claims 1, 6, 7 and 12 nor does the modification as suggested by the Examiner.

Additionally, nothing in *Burr* shows, teaches or suggests that the EIB-MOS transistor comprises a EIB-DTMOS transistor as claimed in claims 2 and 8. Furthermore, nothing in *Burr* shows, teaches or suggests that the EIB-MOS transistor comprises a EIB-VTMOS transistor as claimed in claims 4 and 10 or that the MOS transistor is included in a CMOS circuit as one of a pair of EIB-MOS transistors as claimed in claims 5 and 11.

For all of the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's rejection of claims 1, 2, 4-6, 7, 8 and 10-12 under 35 U.S.C. § 103.

IX. Applicants arguments against the rejection of claims 3 and 9 under 35 U.S.C. § 103

A. Errors in the Rejection

It is respectfully submitted that the rejection of claims 3 and 9 is erroneous because the difference between the claimed subject matter and the cited prior art is such that the

invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. It is respectfully submitted that the Examiner is only selecting bits and pieces from the references without considering the remaining teachings of those references which would lead away from the claimed invention. Furthermore, it is respectfully submitted that the Examiner is misinterpreting *Burr* and impermissibly modifying *Warashina et al.* in light of Applicants' teachings.

B. Limitations Not Described in the Prior Art

The limitation not described in the prior art is that the EIB-DTMOS transistor comprises an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that the channel has the same conductivity type as that of carriers introduced into the channel as claimed in claims 3 and 9.

C. Explanation of Why the Limitations Render the Claimed Subject Matter Unobvious Over the Prior Art

As discussed above, *Burr* does not show, teach or suggest a) a surrounded or body region including a depletion layer having a composition surface which is in contact with the insulating layer, b) a EIB-MOS transistor or c) a substrate of the EIB-MOS transistor is applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the surrounded or body region as claimed in claims 1 and 7.

Warashina et al. relates to a method of manufacturing a semiconductor device for forming an insulated gate field effect transistor in a completely isolated SOI layer, and has for its object to prevent depletion or inversion surely by introducing impurities of sufficiently high concentration into an SOI layer adjacent to an isolating film filled up between element regions of the SOI layer and a backing insulating layer and to aim at flattening of the SOI substrate surface, and further, includes the steps of implanting impurity ions into a semiconductor layer from an oblique direction so as to reach the semiconductor layer under an oxidation-preventive mask using the oxidation-preventive mask as a mask for ion implantation, heating the semiconductor layer in an oxidizing

atmosphere with the oxidation-preventive mask so as to form a local oxide film to isolate the semiconductor layer, and also forming a impurity region with impurities implanted into the semiconductor layer in a region adjacent to the local oxide film and to at least an insulating layer under the semiconductor layer.

Thus, *Warashina* merely discloses completely isolating adjacent element regions from each other by an isolating film filled between the element regions of a SOI layer. Nothing in *Warashina et al.* shows, teaches or suggests a) a surrounded or body region including a depletion layer having a composition surface which is in contact with the insulating layer, b) a EIB-MOS transistor, c) a substrate applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the surrounded or body region or d) a EIB-DTMOS transistor comprising an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that the channel has the same conductivity type as that of carriers introduced into the channel as claimed in claims 3 and 9. Rather, *Warashina et al.* merely discloses completely isolating adjacent element regions from each other by an isolating film fitted between the element regions of a SOI layer.

D. Why the References Taken as a Whole do not Suggest the Claimed Invention and Why the Features Disclosed in One Reference May Not Be Properly Combined With the Features Disclosed in the Other Reference

As discussed above, nothing in *Burr* or *Warashina et al.* show, teach or suggest a) a surrounded or body region including a depletion layer having a composition surface which is in contact with the insulating layer, b) a EIB-MOS transistor, c) a substrate applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the body or surrounded region or d) a EIB-DTMOS transistor comprising an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that the channel has the same conductivity type as that of carriers introduced into the channel as claimed in claims 3 and 9. Thus, since neither reference

show, teach or suggest the invention as claimed in claims 3 and 9, the combination thereof will not show, teach or suggest the invention as claimed.

For all of the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's rejection of claims 3 and 9 under 35 U.S.C. § 103.

X. Conclusions

For all of the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case, since it is respectfully submitted that the final rejection of claims 1-12 is in error. Therefore, it is respectfully submitted that claims 1-12 should be allowed.

Respectfully submitted,

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Date: June 18, 2002

APPENDIX A

The Appealed Claims

1. A MOS transistor with a controlled threshold voltage, comprising:

a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer,

said single crystal layer being formed therein with a source region, a drain region and a surrounded region surrounded by said source region and said drain region,

said surrounded region including a depletion layer having a composition surface which is in contact with said insulating layer,

said MOS transistor comprising an EIB-MOS transistor of which said substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over said composition surface of the surrounded region.

2. The MOS transistor according to claim 1, wherein said EIB-MOS transistor comprises an EIB-DTMOS transistor.

3. The MOS transistor according to claim 2, wherein said EIB-DTMOS transistor comprises an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that said channel has the same conductive type as that of carriers introduced into said channel.

4. The MOS transistor according to claim 1, wherein said EIB-MOS transistor comprises an EIB-VTMOS transistor.

5. The MOS transistor according to claim 1, included in a CMOS circuit as one of pair of EIB-MOS transistors.

6. A method of controlling a threshold voltage of a MOS transistor with a controlled threshold voltage, said MOS transistor being an EIB-MOS transistor and

comprising a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer, said single crystal layer being formed therein with a source region, a drain region and a surrounded region surrounded by said source region and said drain region, said surrounded region including a depletion layer having a composition surface which is in contact with said insulating layer, wherein said method comprises the step of applying a voltage of a first polarity to said substrate for inducing charges of a second polarity over said composite surface of the surrounded region.

7. A MOS transistor with a threshold voltage controlled by changing a body potential of the MOS transistor, comprising:

a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer,

said single crystal layer being formed therein with a source region, a drain region and a body region surrounded by said source region and said drain region,

said body region including a depletion layer having a composition surface which is in contact with said insulating layer,

said MOS transistor comprising an EIB-MOS transistor of which said substrate is applied with a voltage of a first polarity for inducing charges of a second polarity over said composition surface of the body region.

8. The MOS transistor according to claim 7, wherein said EIB-MOS transistor comprises an EIB-DTMOS transistor.

9. The MOS transistor according to claim 8, wherein said EIB-DTMOS transistor comprises an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that said channel has the same conductive type as that of carriers introduced into said channel.

10. The MOS transistor according to claim 7, wherein said EIB-MOS transistor comprises an EIB-VTMOS transistor.

11. The MOS transistor according to claim 7, included in a CMOS circuit as one of pair of EIB-MOS transistors.

12. A method of controlling a threshold voltage of a MOS transistor by changing a body potential of the MOS transistor, said MOS transistor being an EIB-MOS transistor and comprising a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between said substrate and said single crystal layer, said single crystal layer being formed therein with a source region, a drain region and a body region surrounded by said source region and said drain region, said body region including a depletion layer having a composition surface which is in contact with said insulating layer, wherein said method comprises the step of applying a voltage of a first polarity to said substrate for inducing charges of a second polarity over said composition surface of the body region.

APPENDIX B

Figs. 5-11

FIG. 5

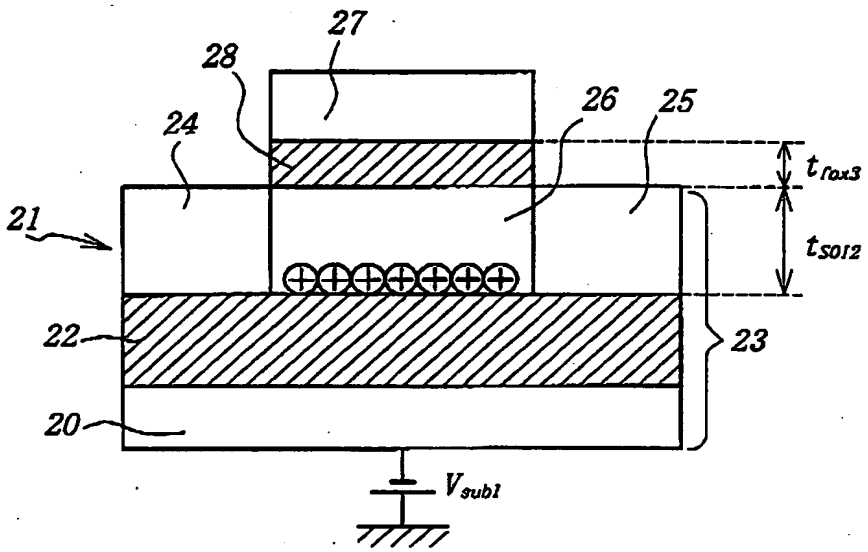


FIG. 6

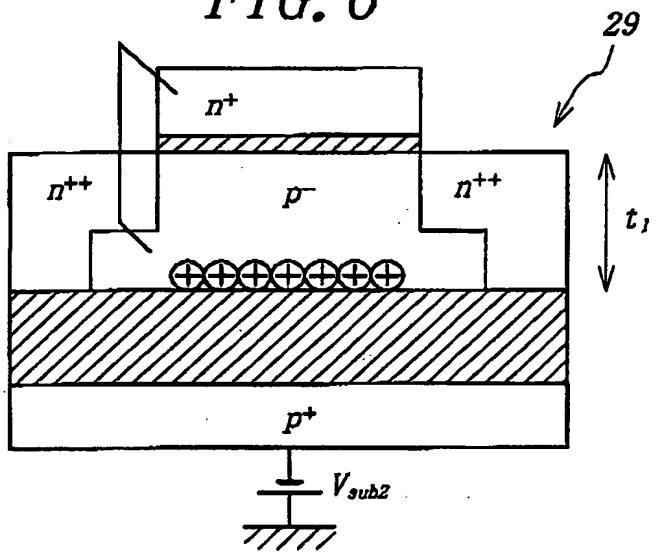
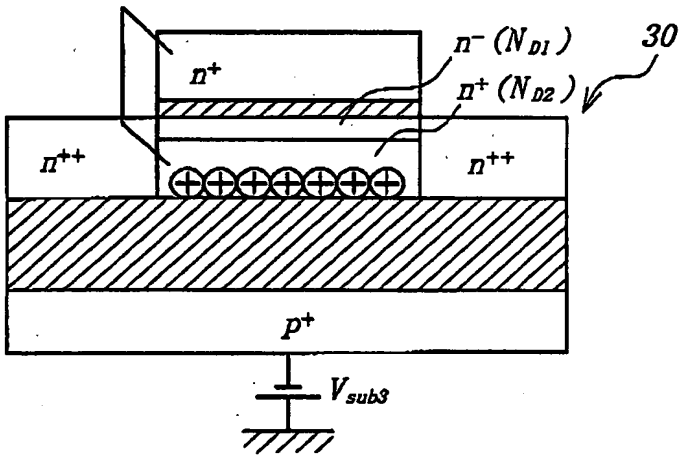


FIG. 7



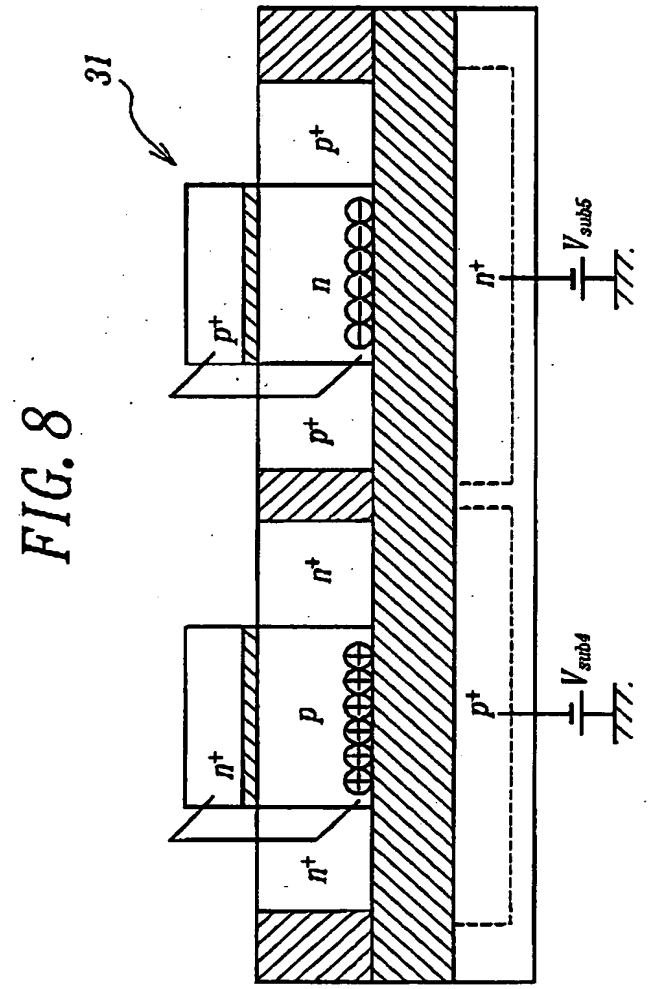


FIG. 8

FIG. 9

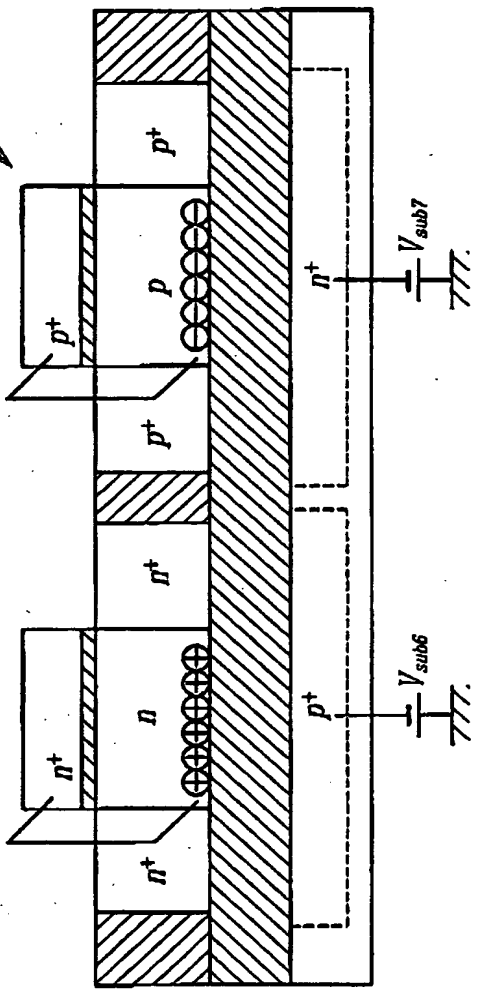
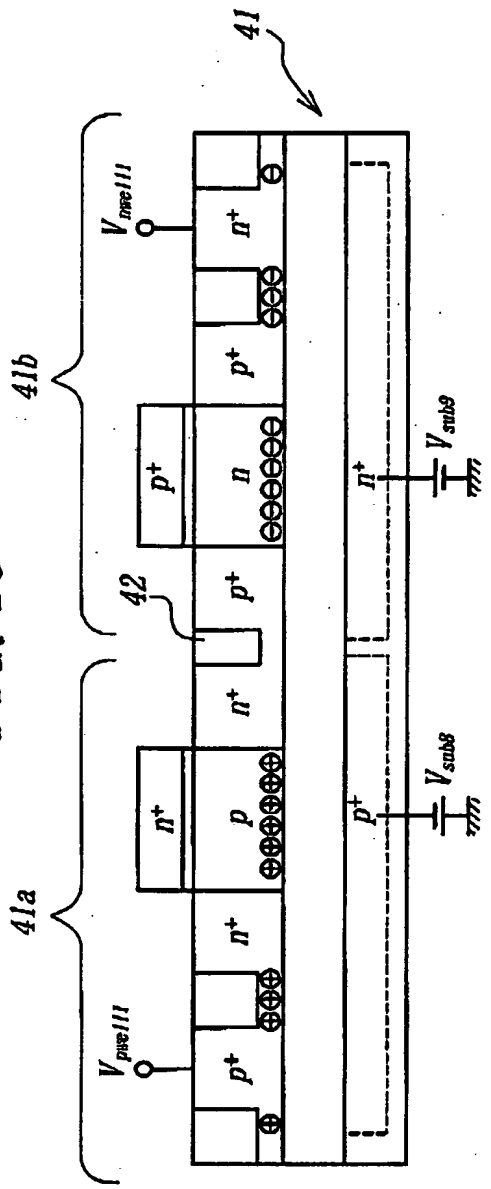


FIG. 10


41
41b
41a
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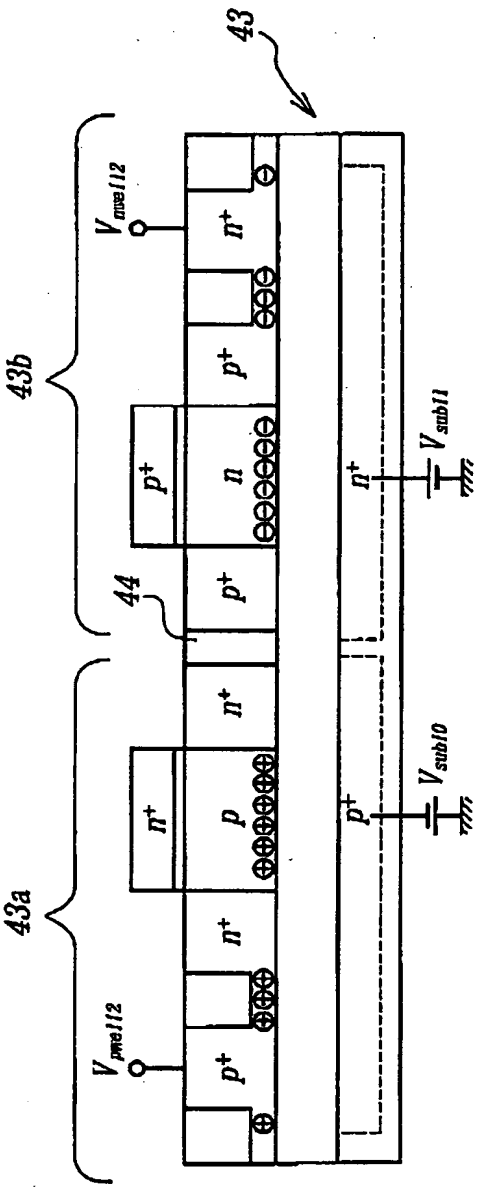
V_{pwe111}
V_{pwe111}
V_{sub9}
V_{sub8}
p^+
n^+
n
p

FIG. 11


43
43b
43a
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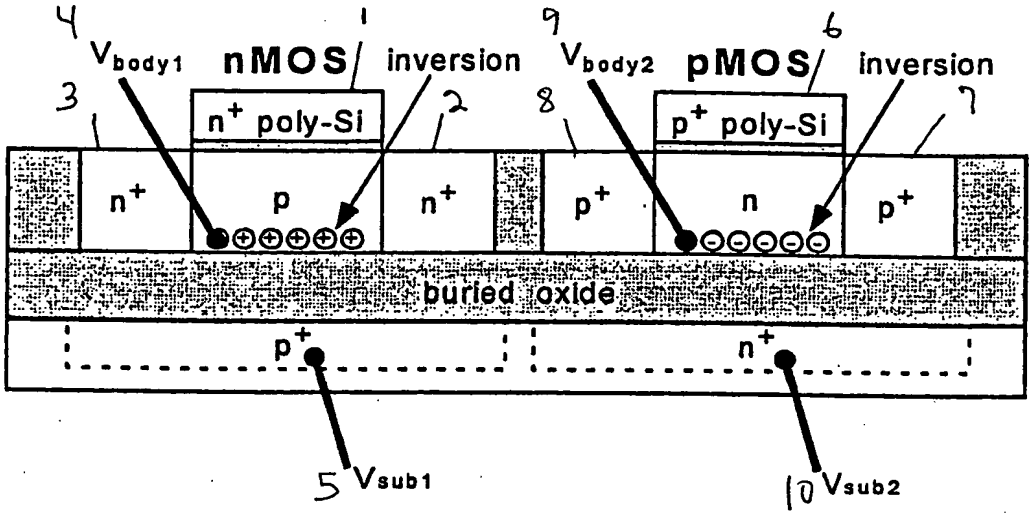
n
p

APPENDIX C

(a) Present Invention



(b) Burr